**ASSIGNMENT-1**

**SUBJECT: APPLIED PHYSICS**

**TOPIC: DC POWER SUPPLY**



**Submitted to: Sir Irfan**

**Submitted by: Shahzad Akbar**

**Major: BSCS**

**Roll No: 0233-BSCS-22**

**SECTION: CSE1**

**GC UNIVERSITY LAHORE**

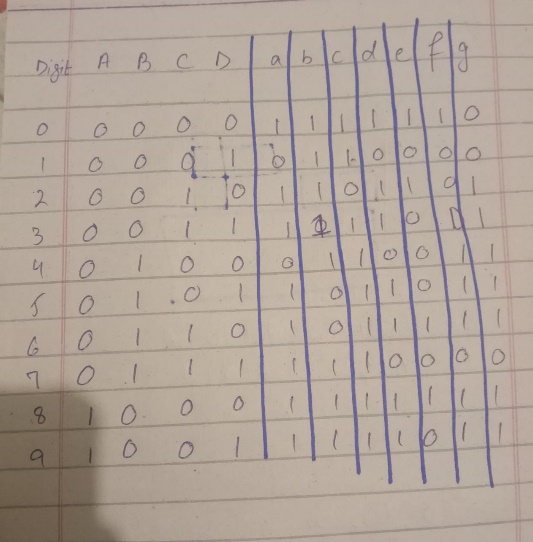
**Introduction:**

In the realm of digital logic design, 7-segment displays stand as essential tools for visually conveying numeric information. Comprising seven LED segments in a distinctive pattern, these displays can represent numbers, letters, and basic symbols. By delving into the principles governing their operation, encoding methods, and integration with digital systems, we can uncover their significance in various applications, from digital clocks to industrial equipment. In this assignment, we'll explore the inner workings of 7-segment displays and the role they play in bridging the gap between binary data and human-readable information, showcasing their vital role in the world of digital logic design.

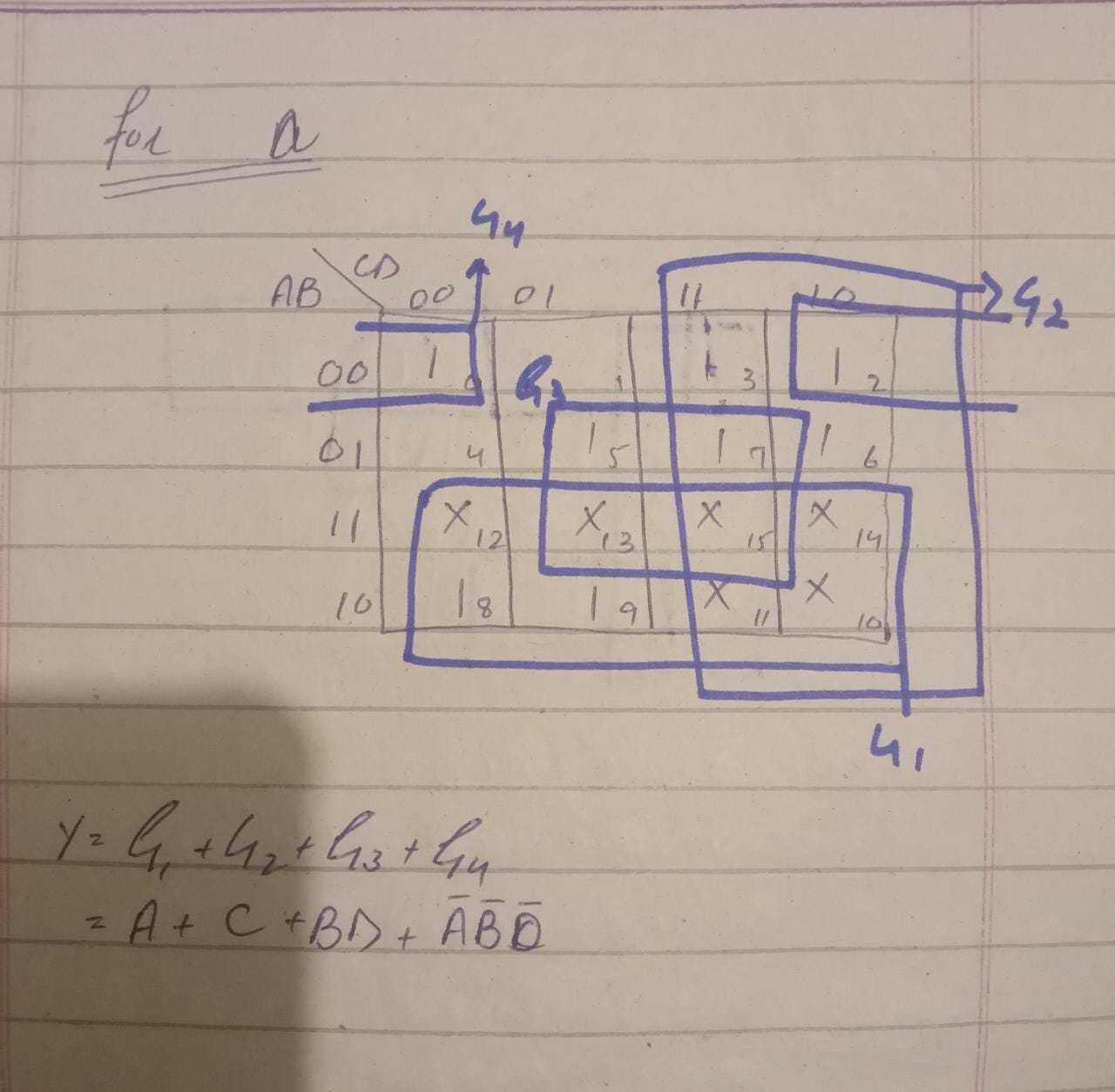
**Objective:**

The objective of this assignment is to provide a comprehensive understanding of 7-segment displays in the context of digital logic design. Through exploration of their construction, operation, encoding techniques, and integration within digital systems, students will gain insights into how these displays facilitate the visual representation of numeric data. By the end of this assignment, learners will be equipped with the knowledge to comprehend the significance of 7-segment displays and their applications in conveying information within various digital circuits and devices.

**Methodologies:**

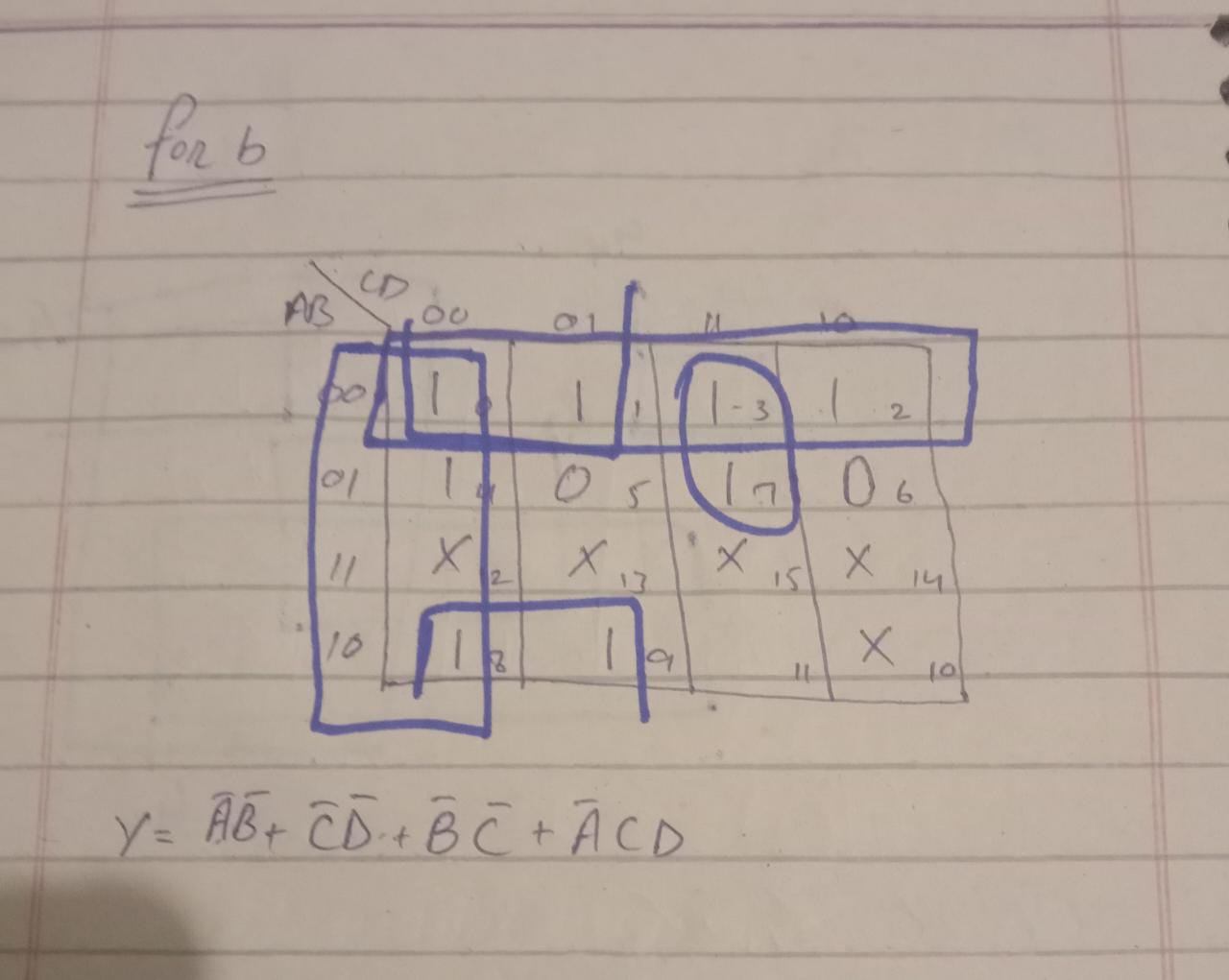
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**Working of a:**

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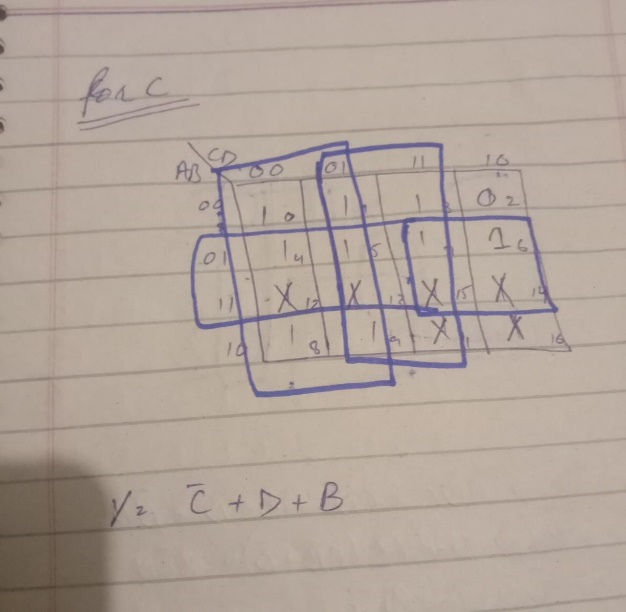
**a = A + C + BD + A’B’D’**

**Working of b:**

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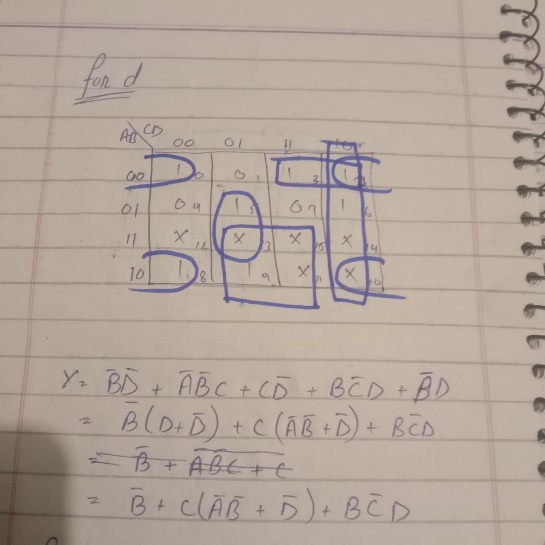
**b = A’B’ + C’D’ + B’C’ + A’CD**

**Working of c:**

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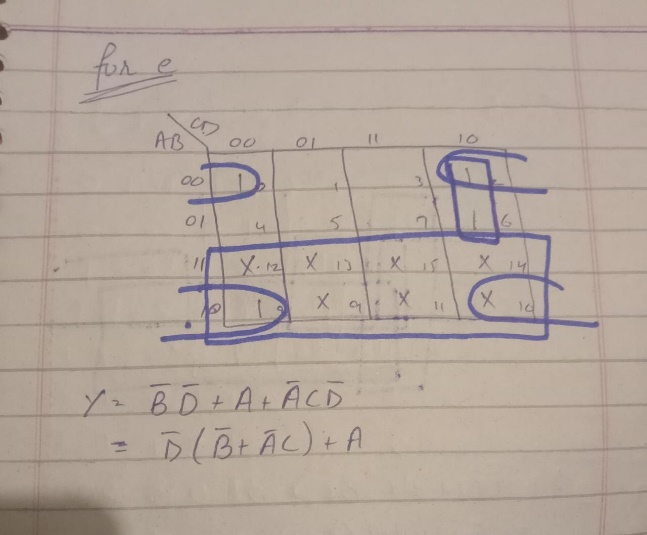
**c = C’ + D + B**

**Working of d:**

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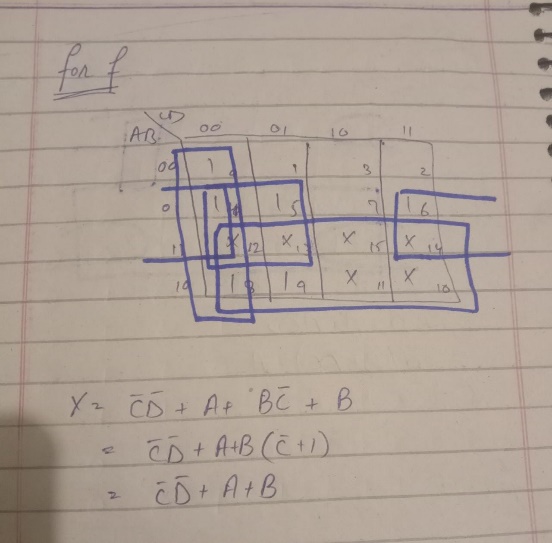
**d = B’ + C(A’B’ + D’) + BC’D**

**Working of e:**

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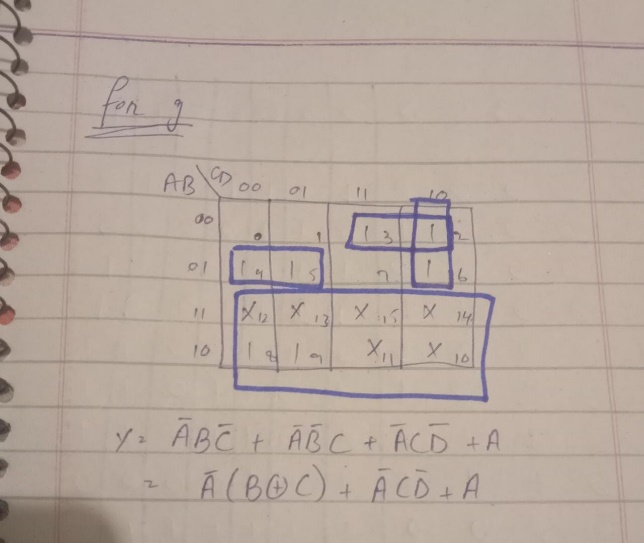
**e = D’(B’ + A’C) + A**

**Working of f:**

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**f = C’D’ + A + B**

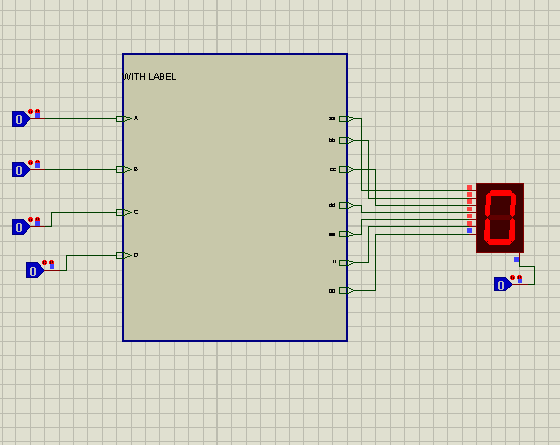
**Working of g:**

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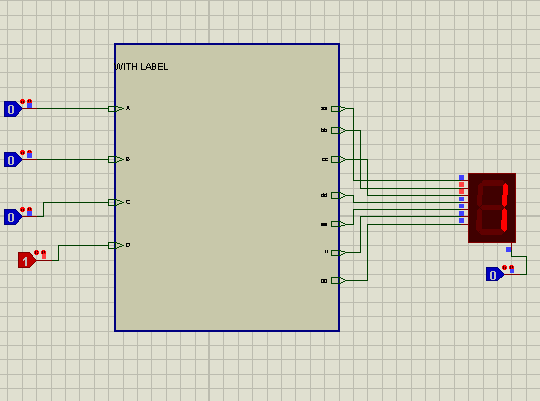
**g = A’(B XOR C) + A’CD’ + A**

**Results:**

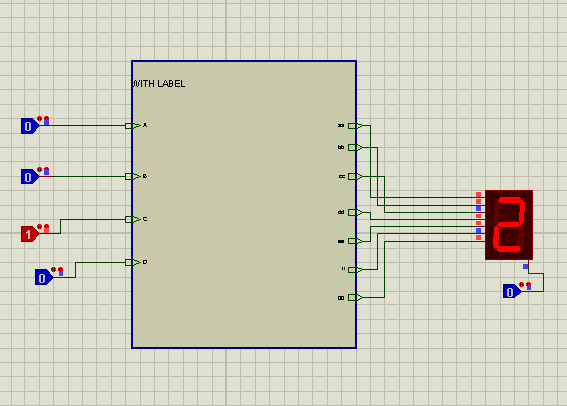
**Working of 0:**

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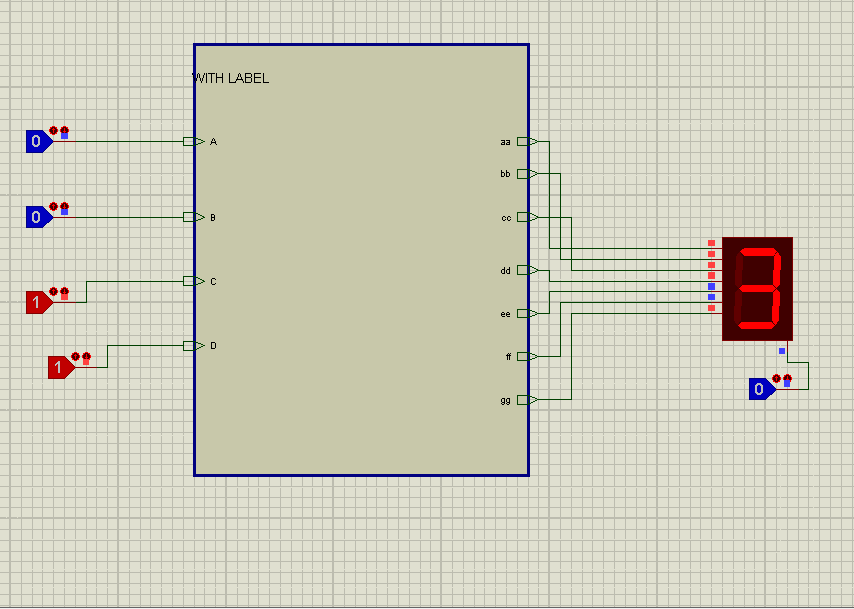
**Working of 1:**

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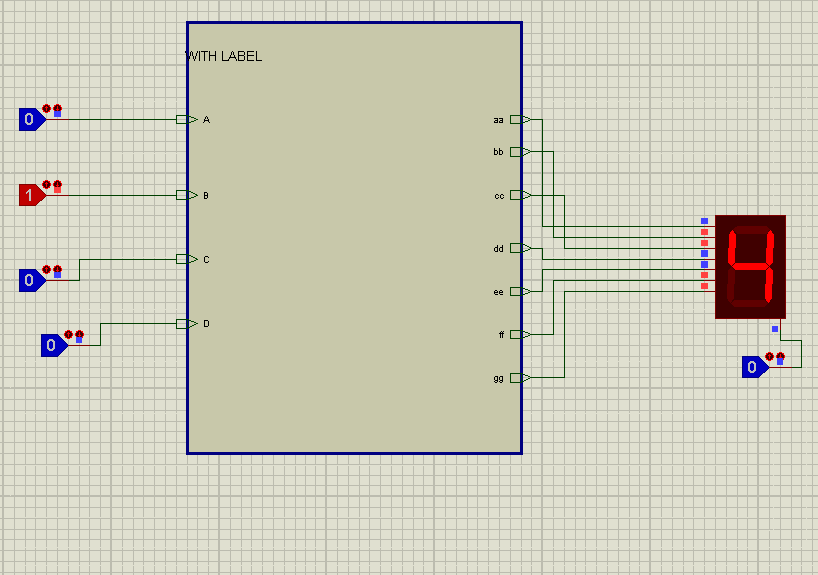
**Working of 2:**

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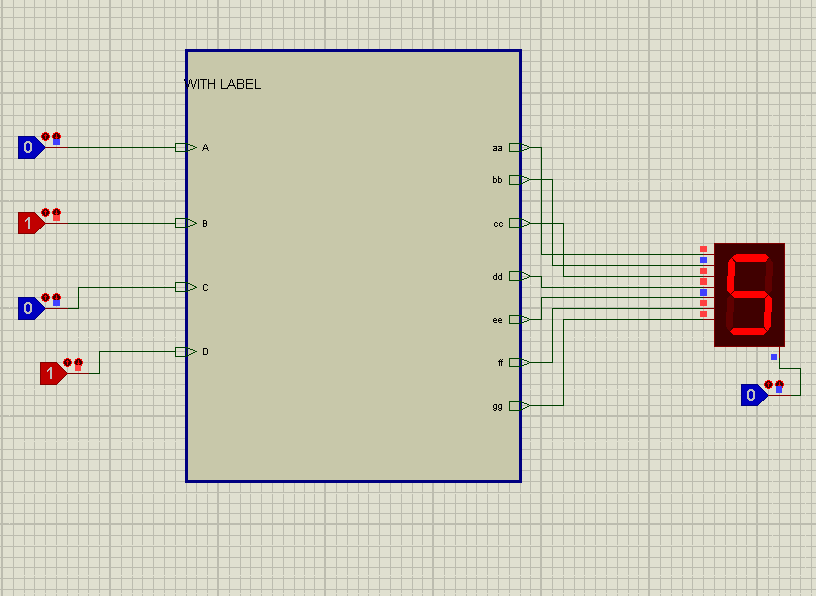
**Working of 3:**

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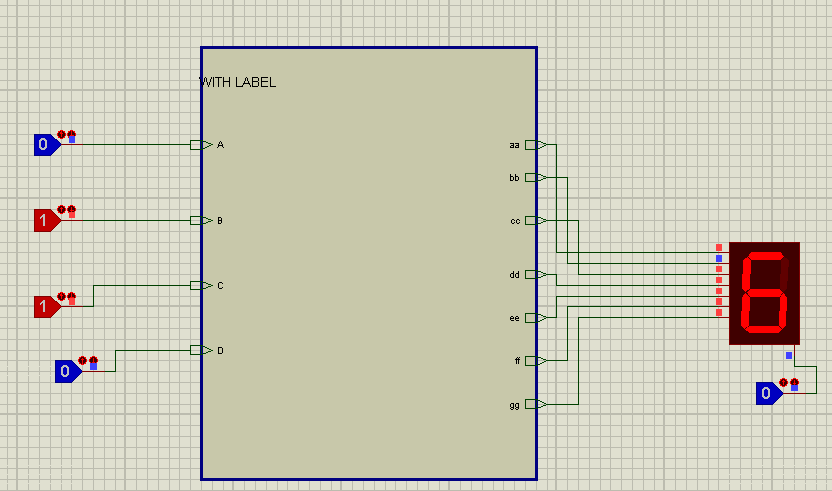
**Working of 4:**

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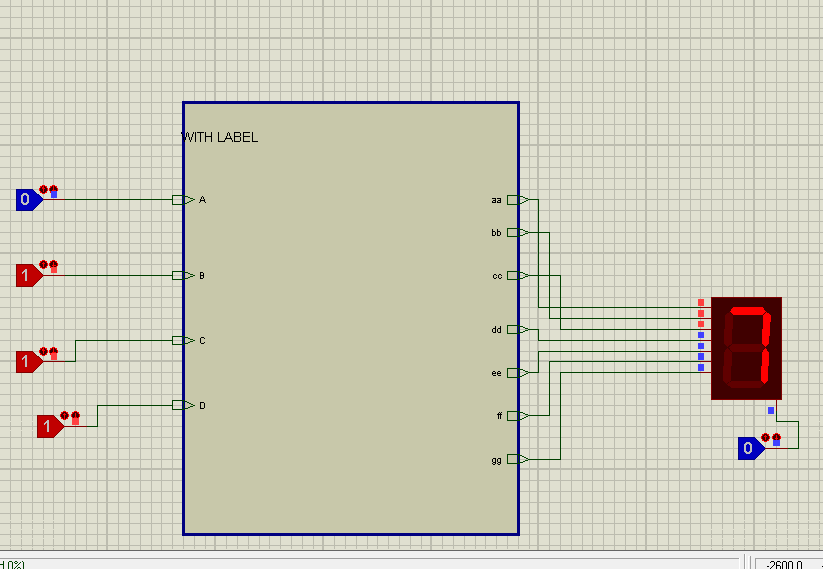
**Working of 5:**

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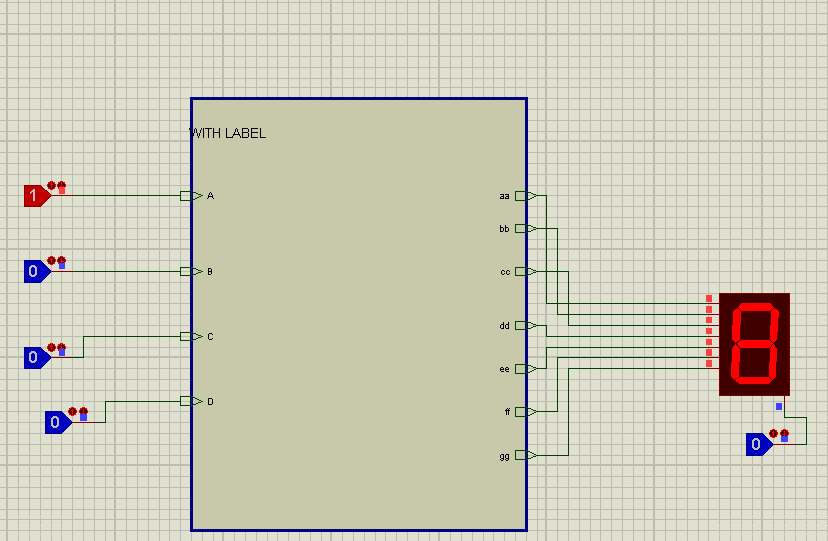
**Working of 6:**

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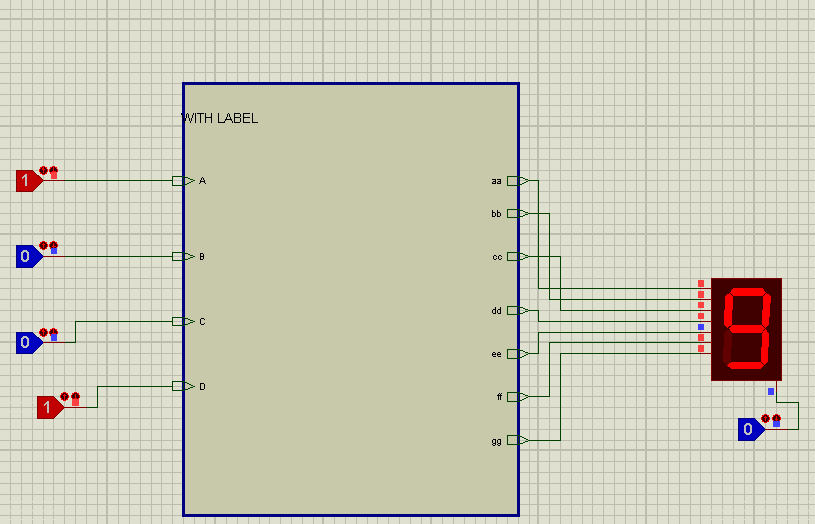
**Working of 7:**

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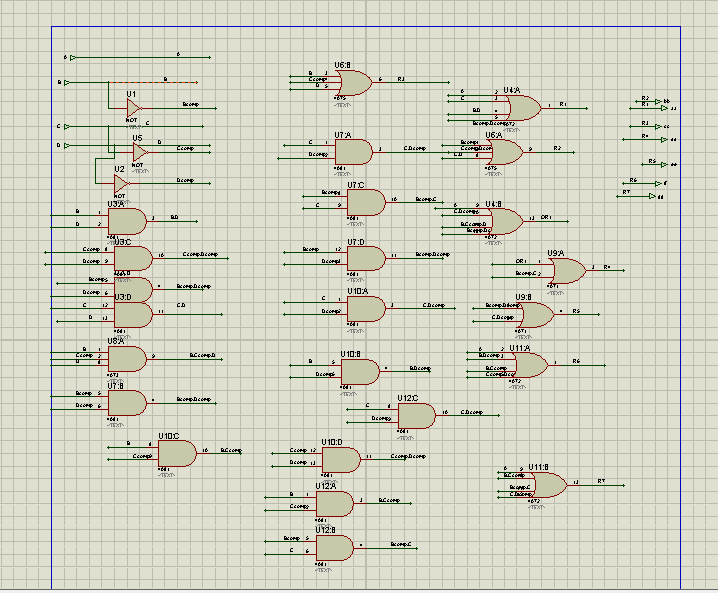
**Working of 8:**

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**Working of 9:**

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**Circuit Explanations:**

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A circuit made for IC package of BCD-7SEG. For a; A + C + BD + A’B’D’

Equation is drawn using K-Map and mapped upon the circuit.

For b; A’B’ + C’D’ + B’C’ + A’CD Equation is drawn using K-Map and mapped upon the circuit.

For c; C’ + D + B, Equation is drawn using K-Map and mapped upon the circuit.

For d; B’ + C(A’B’ + D’) + BC’D, Equation is drawn using K-Map and mapped upon the circuit.

For e; D’(B’ + A’C) + A, Equation is drawn using K-Map and mapped upon the circuit.

For f; C’D’ + A + B, Equation is drawn using K-Map and mapped upon the circuit.

For g; A’(B XOR C) + A’CD’ + A, Equation is drawn using K-Map and mapped upon the circuit.